



# **DesignWare**

## **minPower Components**

### **Documentation Overview**



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# DesignWare minPower Components Documentation Overview

DesignWare minPower Components comprise a low power, technology-independent, microarchitecture-level library that is tightly integrated into the Synopsys synthesis environment.

The following sections list the documentation set and datasheets that support this library:

- [“DesignWare minPower Components Document List”](#) on page 3
- [“List of DesignWare minPower Components”](#) on page 4

## 1.1 DesignWare minPower Components Document List

Table 1-1 DesignWare minPower Components Documentation

<a href="#">DesignWare minPower Components Release Notes</a> manuals/minpower_relnotes.pdf	Contains usage issues for DesignWare minPower Components Library (F-2011.09) for Design Compiler 201109.0.
<a href="#">DesignWare minPower Components User Guide</a> manuals/minpower_userguide.pdf	Explains the use of DesignWare minPower Components. NOTE: The <i>DesignWare minPower Application Notes</i> document is now <a href="#">Appendix A</a> of this User Guide.
<a href="#">DesignWare IP Family Reference Guide</a> <a href="https://www.synopsys.com/dw/doc.php/doc/dwf/manuals/dw_frg.pdf">https://www.synopsys.com/dw/doc.php/doc/dwf/manuals/dw_frg.pdf</a>	Provides general information for most DesignWare Synthesizable and Verification IP.
<a href="#">DesignWare Building Block Quick Reference</a> <a href="https://www.synopsys.com/dw/doc.php/doc/dwf/manuals/dwbb_qrg.pdf">https://www.synopsys.com/dw/doc.php/doc/dwf/manuals/dwbb_qrg.pdf</a>	Provides a brief pin and parameter descriptions for all the DesignWare minPower Components in a single document.
<a href="#">DesignWare minPower Components Overview</a> datasheets/minpower_overview.pdf	Describes the Basic Library components, which provide basic implementations of common arithmetic functions that can be referenced by HDL operators in your VHDL or Verilog source code.

### 1.1.1 List of DesignWare minPower Components

The following table provides links to each datasheet. New IP (2010.12 and later) are indicated with a **New** label.

**Table 1-2 List of DesignWare minPower Components**

IP	Description
<b>minPower Pipelined Floating Point Components</b> ( <a href="#">Overview</a> )	
<a href="#">DW_lp_piped_fp_add</a>	Low Power Pipelined Floating Point Adder ( <b>Enhanced</b> )
<a href="#">DW_lp_piped_fp_div</a>	Low Power Pipelined Floating Point Divide
<a href="#">DW_lp_piped_fp_mult</a>	Low Power Pipelined Floating Point Multiplier
<a href="#">DW_lp_piped_fp_recip</a>	Low Power Pipelined Floating Point Reciprocal
<a href="#">DW_lp_piped_fp_sum3</a>	Low Power Pipelined 3-input Floating Point Adder
<b>minPower Components with Datapath Gating</b> ( <a href="#">Overview</a> )	
<a href="#">DW_fp_add_DG</a>	Low Power Point Adder with Datapath Gating
<a href="#">DW_fp_addsub_DG</a>	Low Power Floating Point Adder/Subtractor with Datapath Gating
<a href="#">DW_fp_cmp_DG</a>	Low Power Floating Point Comparator with Datapath Gating
<a href="#">DW_fp_div_DG</a>	Low Power Floating Point Divide with Datapath Gating
<a href="#">DW_fp_mac_DG</a>	Low Power Floating Point Multiply-and-Add with Datapath Gating
<a href="#">DW_fp_mult_DG</a>	Low Power Floating Point Multiplier with Datapath Gating
<a href="#">DW_lp_fp_multifunc_DG</a>	Low Power Floating Point Multi-Function Unit with Datapath Gating ( <b>New</b> )
<a href="#">DW_lp_multifunc_DG</a>	Low Power Multi-Function Unit with Datapath Gating ( <b>New</b> )
<a href="#">DW_fp_recip_DG</a>	Low Power Floating Point Reciprocal with Datapath Gating
<a href="#">DW_fp_sub_DG</a>	Low Power Floating Point Subtractor with Datapath Gating
<a href="#">DW_fp_sum3_DG</a>	Low Power 3-input Floating Point Adder with Datapath Gating
<b>minPower FIFO Controllers</b> ( <a href="#">Overview</a> )	
<a href="#">DW_lp_fifoctrl_1c_df</a>	Low Power Single-clock FIFO Controller with Dynamic Flags
<b>minPower Arithmetic Components</b> ( <a href="#">Overview</a> )	
<a href="#">DW_lp_cntr_up_df</a>	Low Power “Up” Counter with Dynamic Terminal Count Flag ( <b>New</b> )
<a href="#">DW_lp_cntr_updn_df</a>	Low Power “Up/Down” Counter with Dynamic Terminal Count Flag ( <b>New</b> )
<a href="#">DW_lp_multifunc</a>	Low Power Fixed-Point Multi-Function Unit
<a href="#">DW_lp_fp_multifunc</a>	Low Power Floating-Point Multi-Function Unit
<a href="#">DW_lp_pipe_mgr</a>	Low Power Pipeline Manager
<a href="#">DW_lp_piped_div</a>	Low Power Pipelined Divider
<a href="#">DW_lp_piped_ecc</a>	Low Power Pipelined Error Correction Code (ECC)

**Table 1-2 List of DesignWare minPower Components (Continued)**

IP	Description
<a href="#">DW_lp_piped_mult</a>	Low Power Pipelined Multiplier
<a href="#">DW_lp_piped_prod_sum</a>	Low Power Pipelined Sum of Products
<a href="#">DW_lp_piped_sqrt</a>	Low Power Pipelined Square Root

### 1.1.2 List of minPower Enhanced Library Components

The following table provides links to Low Power Library datasheets. These existing components use the minPower license (DesignWare-LP) to enable low power features. New IP are indicated with a **New** label.

**Table 1-3 List of DesignWare minPower Components**

IP	Description
<b>Enhanced pre-existing IP that have enhanced Clock Gating</b>	
<a href="#">DW03_bictr_dcnto</a>	Up/Down Binary Counter with Dynamic Count-to Flag (Enhanced)
<a href="#">DW03_bictr_scnto</a>	Up/Down Binary Counter with Static Count-to Flag (Enhanced)
<a href="#">DW_arb_dp</a>	Arbiter with Dynamic Priority Scheme (Enhanced)
<a href="#">DW_arb_sp</a>	Arbiter with Static Priority Scheme (Enhanced)
<a href="#">DW_fifocntl_s1_df</a>	Synchronous Single-clock FIFO Controller with Dynamic Flags
<a href="#">DW_asymfifocntl_s1_df</a>	Asymmetric I/O Synchronous Single-clock FIFO Controller - Dynamic Flags
<a href="#">DW_fifocntl_s1_sf</a>	Synchronous Single-clock FIFO Controller with Static Flags
<a href="#">DW_asymfifocntl_s1_sf</a>	Asymmetric I/O Synchronous Single-clock FIFO Controller - Static Flags
<a href="#">DW_fifocntl_s2_sf</a>	Synchronous Dual-clock FIFO Controller with Static Flags
<a href="#">DW_asymfifocntl_s2_sf</a>	Asymmetric Synchronous Dual-clock FIFO Controller - Static Flags
<a href="#">DW_fifocntl_2c_df</a>	Synchronous Dual-clock FIFO Controller with Dynamic Flags
<a href="#">DW03_shftreg</a>	Shift Register
<a href="#">DW_dpll_sd</a>	Digital Phase Locked Loop
<a href="#">DW_stackctl</a>	Synchronous (Single Clock) Stack Controller
<a href="#">DW_cntr_gray</a>	Gray Code Counter
<a href="#">DW_mult_seq</a>	Sequential Multiplier
<a href="#">DW_div_seq</a>	Sequential Divider
<a href="#">DW_sqrt_seq</a>	Sequential Square Root
<b>Enhanced pre-existing IP that have Datapath Gating</b>	
<a href="#">DW_piped_mac</a>	Pipelined Multiplier-Accumulator
<a href="#">DW_8b10b_enc</a>	8b10b Encoder
<a href="#">DW_8b10b_dec</a>	8b10b Decoder

**Table 1-3 List of DesignWare minPower Components**

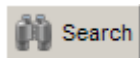
IP	Description
<a href="#">DW_mult_pipe</a>	Stallable Pipelined Multiplier
<a href="#">DW_div_pipe</a>	Stallable Pipelined Divider
<a href="#">DW_sqrt_pipe</a>	Stallable Pipelined Square Root
<a href="#">DW_prod_sum_pipe</a>	Stallable Pipelined Generalized Sum of Products
<a href="#">DW_mult_seq</a>	Sequential Multiplier
<a href="#">DW_div_seq</a>	Sequential Divider
<a href="#">DW_sqrt_seq</a>	Sequential Square Root
<a href="#">DW_fp_div_seq</a>	Floating Point Sequential Divider

## 1.2 Synopsys Common Licensing (SCL)

You can find general SCL information on the following page:

<http://www.synopsys.com/Support/Licensing>

## 1.3 Searching PDF Files



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You can find in an individual PDF file located on a web server or on your local file system; however, in order to search through a collection of PDF files, those files must reside on your local file system.

In addition, many collections of PDF files provided by Synopsys are preconfigured with a search index file called INDEX.PDX, which enables even faster search operations. If an INDEX.PDX file is available, the Adobe Reader locates the file automatically for use in the next search operation.

## 1.4 Additional Information

For additional Synopsys documentation, refer to the following location:

<http://www.synopsys.com/products/designware/docs>

For up-to-date information about the latest verification models and synthesizable IP available from Synopsys, visit the DesignWare IP homepage:

<http://www.designware.com>

From this page you can “Search for IP” in the Search Tools field.